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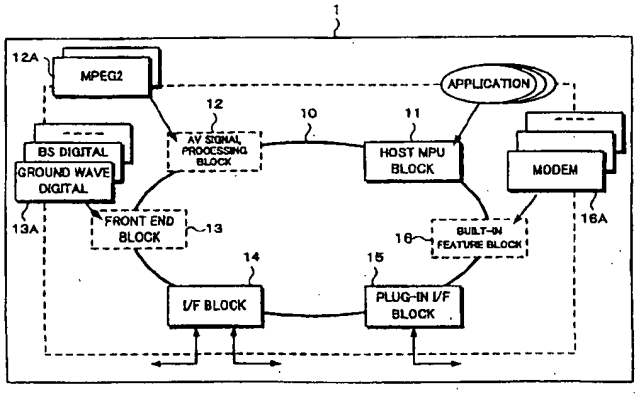
(54) METHOD AND APPARATUS FOR DIGITAL SIGNAL PROCESSING AND METHOD OF PROVIDING EXTENSION FUNCTION

(57) Elements necessary for a digital television receiver are structured as blocks that are a plurality of digital signal processing blocks and a host arithmetic operation processing block. The blocks are connected through a general-purpose bus. Commands for controlling operations of the blocks and data of streams are transferred through the bus. An extension plug-in card for a new service can be attached and detached to / from the bus. The extension plug-in card has hardware that accomplishes an extension function and a script for commands of the hardware. When the extension plug-in card is attached to the bus through an interface, the script for the commands is automatically uploaded to the host arithmetic operation processing block side. The host arithmetic operation processing block can operate the extension plug-in card corresponding to the transferred script for the commands.

Fig. 2



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ware and issue commands to the hardware. To allow the host MPU to issue commands to the hardware, software may have to be installed to the host MPU. The install work for the software may be troublesome for non-experienced users of television receivers.

[0016] Therefore, an object of the present invention is to provide a digital signal processing apparatus, a system thereof, and an extension function providing method that allow hardware for an extended function to be easily connected to a bus for a device of which required functions are structured as blocks and connected through a standardized bus.

Disclosure of the Invention

[0017] The present invention is a digital signal processing apparatus, comprising:

a plurality of digital signal processing blocks and a host arithmetic operation processing block as functions necessary for processing a digital signal;
a bus for connecting the host arithmetic operation processing block and the plurality of digital signal processing blocks; and
an interface for an extension function providing medium connected to the bus,
wherein the extension function providing medium has:

a means for accomplishing an extension function; and
a script embedding a command for operating the extension function, and
wherein when the extension function providing medium is attached to the bus through the interface, the script is sent to the host arithmetic operation processing block side and a function of the extension function providing medium is operated corresponding to the command embedded in the script.

[0018] The present invention is a digital signal processing system, comprising:

a digital signal processing apparatus having:

a plurality of digital signal processing blocks and a host arithmetic operation processing block as functions necessary for processing a digital signal,
a bus for connecting the host arithmetic operation processing block and the plurality of digital signal processing blocks, and
an interface for an extension function providing medium connected to the bus; and
an extension function providing medium attached to the interface of the extension function providing medium on the digital signal processing side,
wherein the extension function providing medium has:

a means for accomplishing an extension function; and
a script embedding a command for operating the extension function, and
wherein when the extension function providing medium is attached to the bus through the interface, the script is sent to the host arithmetic operation processing block side and a function of the extension function providing medium is operated corresponding to the command embedded in the script.

[0019] The present invention is an extension function providing method, comprising the steps of:

structuring functions necessary for processing a digital signal as a plurality of digital signal processing blocks and a host arithmetic operation processing block;
connecting the host arithmetic operation processing block and the plurality of digital signal processing blocks through a bus; and
providing an interface for an extension function providing medium connected to the bus,
wherein the extension function providing medium has:

a means for accomplishing an extension function; and
a script embedding a command for operating the extension function, and
wherein when the extension function providing medium is attached to the bus through the interface, the script is sent to the host arithmetic operation processing block side and a function of the extension function providing medium is operated corresponding to the command embedded in the script.

[0020] Elements necessary for a digital television receiver are structured as blocks and connected through a general-purpose bus. In addition, an extension plug-in card for a new service can be attached and detached to / from the bus. The extension plug-in card has hardware that accomplishes an extension function and a script that describes a command for controlling the hardware. When the extension plug-in card is attached to the bus through an interface, the script is automatically uploaded to the host arithmetic operation processing block side. The host arithmetic operation processing block can operate the extension plug-in card corresponding to the transferred script. Thus, when new hardware is added, it is not necessary to install software.

blocks 12, 13, and 16 may be connected to the standardized bus. Alternatively, the individual blocks 11, 12, 13, 14, 15, and 16 may be structured as integrated circuits or modules.

[0032] In the above example, the receiver is divided into the host MPU block 11, the AV signal processing block 12, the front end block 13, the interface block 14, the plug-in interface block 15, and the built-in feature block 16. However, it should be noted that the dividing method is not limited to such an example.

[0033] Of course, when each block is disposed on a board, one block is not always composed of one board. In other words, two or more functional blocks may be disposed on one board. For example, the host MPU block 11 and the interface block 14 may be disposed on one board. Of course, one block may be composed of a plurality of boards.

[0034] Each of the block 11, 12, 13, 14, 15, and 16 interprets a command received through the bus 10, executes a process corresponding to the command, and processes a stream and data received through the bus 10.

[0035] Since a command that does not largely depend on hardware is received through the bus 10, each of the blocks 12, 13, 14, 15, and 16 has a CPU (Central Processing Unit) in many cases so as to interpret the received command and process it. The CPU of each of the blocks 12, 13, 14, 15, and 16 interprets a received command and executes a process corresponding to the command. Each of the blocks 12, 13, 14, 15, and 16 has a driver that operates hardware corresponding to the received command. A portion that largely depends on hardware completes a process in the block thereof.

[0036] In other words, as shown in a conceptual diagram shown in Fig. 4, the host MPU block 11 side has a high level interface HIF for a process with a high level command that is a general purpose command and that does not depend on hardware. On the other hand, each of the blocks 12, 13, 14, and 15 side has a driver DRV that interprets a high level command and performs a process that more depends on hardware and a low level interface LIF that directly controls the hardware.

[0037] The host MPU block 11 side sends a high level command through the high level interface HIF and transfers it to each block through the bus 10. The driver DRV of each block interprets a high level command. In that case, portions that depend on hardware are handled by the driver DRV of each of the blocks 12, 13, 14, and 15.

[0038] On the other hand, as shown in Fig. 5, the host MPU block 11 side may have a driver DRV. However, in the case shown in Fig. 5, when new hardware is added or hardware is changed, a new driver DRV should be installed or the existing driver DRV should be changed.

[0039] High speed streams such as streams of video data and audio data and data that is not on real time basis such as commands and data are transferred to the bus 10. A bus that can transfer different types of data may have two bands that are a band for a high speed stream such as video data and audio data and a band for data that is not on real time basis such as commands. Alternatively, data may be assigned priority in such a manner that streams of video data and audio data are assigned high priority so that the streams of video data and audio data are transmitted at high speed.

[0040] A command that is transmitted to the bus 10 is for example a script type command that is not on real time basis unlike a timing control command. Thus, the data amount of a command that is sent can be remarkably suppressed. Consequently, the same bus 10 can send both commands and streams of video data and audio data.

[0041] In such a manner, the digital television receiver is structured in such a manner that the individual blocks 11, 12, 13, 14, 15, and 16 are connected through the bus 10 and commands, streams, and data are exchanged through the bus 10. Thus, the digital television receiver can easily handle various types of television broadcasts. Consequently, the developing environment of the receiver is remarkably improved.

[0042] For example, when a ground wave digital broadcast is started, a television receiver that receives it should be newly developed. However, when the receiver is designed from the beginning as the service the ground wave digital broadcast is started, the developing efficiency of the receiver becomes low.

[0043] Although the carrier frequency, modulating system, error correcting system, transport stream structure, and so forth of the conventional digital satellite broadcasts are different from those of ground wave digital broadcasts, when other systems of the conventional digital satellite broadcasts are the same as those of the ground wave digital broadcasts, only the AV signal processing block 12 and the front end block 13 for the ground wave digital broadcasts can be developed. In that case, as the services of the ground wave digital broadcasts are started, an AV signal processing block 12A for ground wave digital broadcasts and a front end block 13A for ground wave digital broadcasts are developed. When only the AV signal processing block 12 and the front end block 13 are substituted with the AV signal processing block 12A and the front end block 13A, respectively, the television receiver can handle the ground wave digital broadcasts that will be newly started. Thus, it is not necessary to develop a receiver for ground wave digital broadcasts from the beginning. Even if particular portions for ground wave digital broadcasts are required, only those portions can be newly developed. In addition, the operation of the receiver can be changed by changing the application program of the host MPU block 11.

[0044] Likewise, receivers for digital television broadcasts through satellites in European countries and receivers for digital television broadcasts of US CATV stations can be easily developed without need to newly design those receivers from the beginning.

[0045] In CS digital broadcasts, a television receiver

[0061] The AV signal processing block 31 extracts video packets and audio packets from the transport stream and decompresses the video packets and audio packets to original video data and audio data. The AV signal processing block 31 can perform a picture process for the decoded video data.

[0062] The AV signal processing block 31 has a CPU 41, a video decoder 42, an audio decoder 43, a demultiplexer 44, a graphics processing circuit 45, and a bridge circuit 46. The CPU 41, the video decoder 42, the audio decoder 43, the demultiplexer 44, the graphics processing circuit 45, and the bridge circuit 46 are connected to an in-chip bus 47.

[0063] The front end block 32 selects a desired carrier wave signal from the received signal, demodulates the selected carrier wave signal, performs an error correcting process for the demodulated signal, and outputs a transport stream. The front end block 32 has a front end pack 51 and a CPU 52. The front end pack 51 has a mixer circuit, a local oscillating circuit, an intermediate frequency amplifying circuit, a demodulating circuit, an error correcting circuit, and so forth that convert the received signal into an intermediate frequency signal.

[0064] The interface block 33 provides an interface with an external device corresponding to for example the IEEE 1394 standard. The external interface block 33 has an interface 61 corresponding to for example the IEEE 1394 standard and a CPU 62.

[0065] The built-in feature block 34 is used to provide an addition circuit necessary for receiving a digital broadcast. In a digital broadcast, received data is transferred through a telephone line so as to perform a charging process. To do that, a modem is disposed in the built-in feature block 34. The built-in feature block 34 has a circuit 71 that accomplishes an additional function (in this case, a modem) and a CPU 72.

[0066] The plug-in interface 35 provides an extension function for receiving a new service. The extension plug-in card 36 is attached to the plug-in interface 35. The extension plug-in card 36 has an extension function 81 and a CPU 82. The extension function 81 is composed of software and hardware that accomplish an extension function.

[0067] The structure shown in Fig. 7 composes a television receiver 20 that receives for example a digital CS broadcast. In that case, the front end block 32 that performs the QPSK demodulating process, the Viterbi decoding process, and the Reed-Solomon code error correcting process is used. The AV signal processing block 31 that decompresses video packets of transport streams compressed corresponding to the MPEG 2 system and audio packets compressed corresponding to the MPEG system is used.

[0068] In a digital CS broadcast, for example, a signal of 12 GHz band is used. A received signal of 12 GHz band transmitted from a satellite is received by a parabola antenna (not shown). The received signal is converted into a signal of around 1 GHz by a low noise converter disposed in the parabola antenna and sent to the front end block 32. The front end block 32 selects a carrier wave signal of a desired channel from the received signal. The front end block 32 performs the QPSK demodulating process, the Viterbi decoding process, and the Reed-Solomon code error correcting process for the signal so as to decode the received signal to the transport stream.

[0069] At that point, the received channel is selected corresponding to a command sent from the host MPU 21 through the bus 30. The host MPU 21 sends a high layer command such as "Receive a frequency of X channel." through the bus 30. The command is sent from the bus 30 to the CPU 52 of the front end block 32. The CPU 52 interprets the command and generates a control signal for designating the received frequency to a desired carrier wave frequency corresponding to the command. In reality, the CPU 52 generates a control signal of the PLL that composes the local oscillator. As a result, the frequency of the received channel is designated.

[0070] The front end block 32 outputs a transport stream of packets of video data compressed corresponding to the MPEG 2 system and packets of audio data compressed corresponding to the MPEG system. The transport stream is sent to the AV signal processing block 31 through the bus 30. Thereafter, the transport stream is sent from the AV signal processing block 31 to_the demultiplexer 44 through the bridge 46 and the in-chip bus 47. The demultiplexer 44 separates the transport stream into video packets and audio packets. The video packets are sent to the video decoder 42. The audio packets are sent to the audio decoder 43. The video decoder 42 performs the decompressing process for the video data compressed corresponding to the MPEG 2 system so as to decode the video data. The audio decoder 43 performs the decompressing process for the audio data compressed corresponding to the MPEG audio system so as to decode the audio data. The video data decoded by the video decoder 42 is sent to the graphics processing circuit 45 through the in-chip bus 47. The graphics processing circuit 45 performs the picture process for the video data.

[0071] The picture process performed by the graphics processing circuit 45 depends on a command received from the host MPU 21 through the bus 30. A high layer command for example "Reduce (or enlarge) the screen. " is sent from the host MPU 21 through the bus 30. The command is sent from the bus 30 to the CPU 41 through the bridge circuit 46. The CPU 41 interprets the command and generates a control signal for reducing / enlarging the screen in the designated size corresponding to the command. In reality, the CPU 41 sends a timing signal for reducing or enlarging the screen and a command for directly controlling hardware to the graphics processing circuit 45 corresponding to the received high layer command.

[0072] Thus, in that example, the individual functions necessary for structuring the television receiver 20 are

extension plug-in card 36 is uploaded (at step S5). When the command script CMD stored in the extension plug-in card 36 is uploaded, the host MPU 21 recognizes a command for the attached extension plug-in card 36 and performs a process for the attached extension plug-in card 36.

[0088] In Fig. 14, after the command script has been uploaded, when the user performs an operation for the extension plug-in card 36 (at step S11), the script is checked (at step S12). Thereafter, it is determined whether or not the checked result is correct (at step S13). When the checked result is not correct, an alarm is output (at step S14). When the checked result is correct, the script engine SENG interprets the script (at step S15) and issues a command (at step S15). The extension plug-in device is operated corresponding to the command (at step S17).

[0089] In the above-described example, the case that a new extension plug-in card 36 is attached was described. Likewise, when a new block is added to the bus 30, a command script for the new block can be uploaded in the same manner.

[0090] In the above example, a digital broadcast receiving device was described. However, the present invention can be applied to other devices such as a digital VTR.

[0091] According to the present invention, elements necessary for a digital television receiver are structured as blocks and connected through a general-purpose bus. In addition, an extension plug-in card for a new service can be attached and detached to / from the bus. The extension plug-in card has hardware that accomplishes an extension function and a script that describes a command for controlling the hardware. When the extension plug-in card is attached to the bus through an interface, the script is automatically uploaded to the host arithmetic operation processing block side. The host arithmetic operation processing block can operate the extension plug-in card corresponding to the transferred script. Thus, when new hardware is added, it is not necessary to install software.

Industrial Applicability

[0092] As described above, the present invention is particularly suitable for accomplishing a television receiver that receives various types of digital broadcasts that differ in carrier waves, modulating systems, compressing systems, and so forth.

Claims

1. A digital signal processing apparatus, comprising:

   a plurality of digital signal processing blocks and a host arithmetic operation processing block as functions necessary for processing a digital signal;
   a bus for connecting said host arithmetic operation processing block and said plurality of digital signal processing blocks; and
   an interface for an extension function providing medium connected to said bus,
   wherein the extension function providing medium has:

   means for accomplishing an extension function; and
   a script embedding a command for operating the extension function, and
   wherein when the extension function providing medium is attached to said bus through said interface, the script is sent to said host arithmetic operation processing block side and a function of the extension function providing medium is operated corresponding to the command embedded in the script.

2. The digital signal processing apparatus as set forth in claim 1,

   wherein each of said plurality of digital signal processing blocks includes means for interpreting a command received through said bus and executing the command.

3. The digital signal processing apparatus as set forth in claim 1,

   wherein the command is a high layer command that does not depend on hardware and that is not on real time basis.

4. The digital signal processing apparatus as set forth in claim 1,

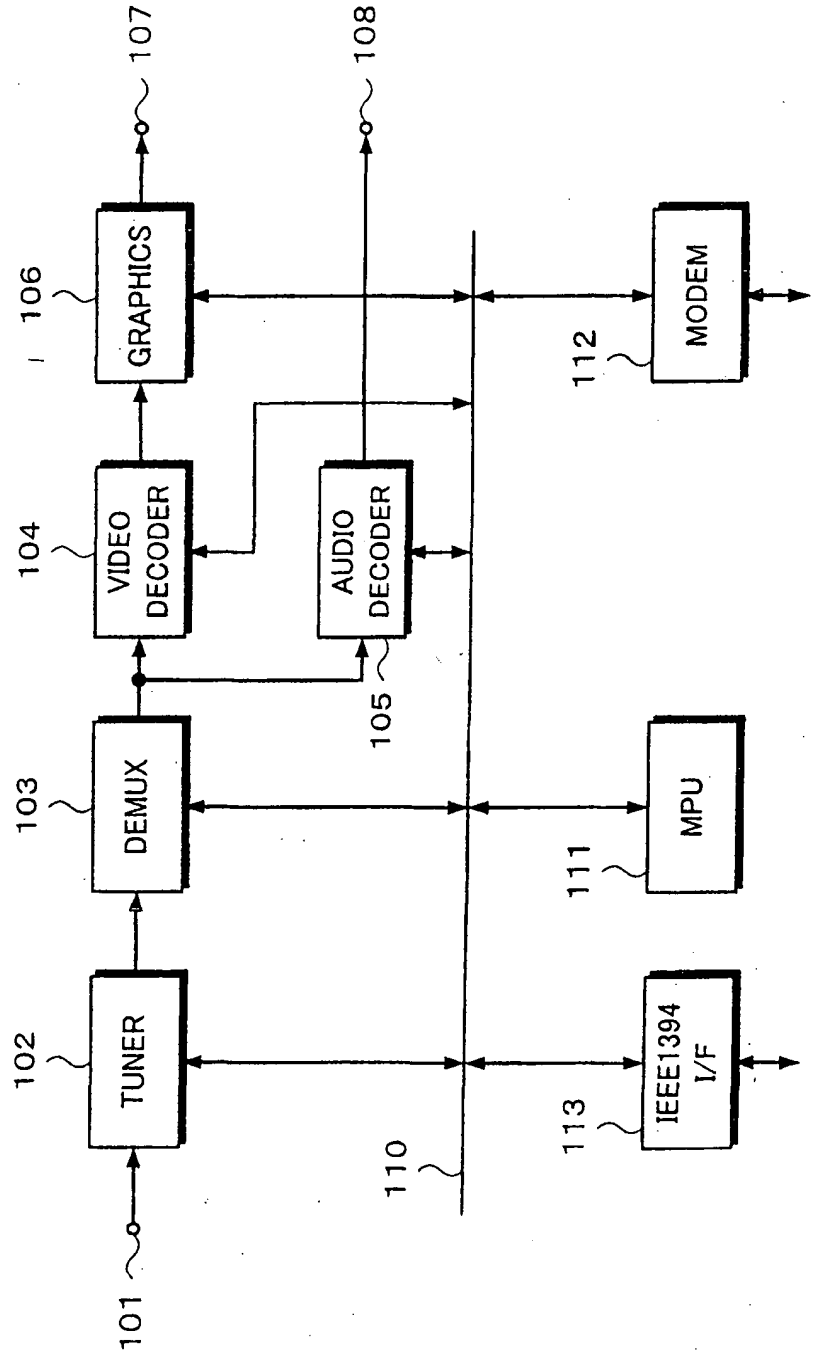
   wherein the command is described and embedded in a script of hypertext,
   wherein the hypertext is interpreted by a browser and a picture for operating the extension function is displayed, and
   wherein a command corresponding to the function is embedded and displayed in the picture for operating the extension function.

5. A digital signal processing system, comprising:

   a digital signal processing apparatus having:

   a plurality of digital signal processing blocks and a host arithmetic operation processing block as functions necessary for processing a digital signal,
   a bus for connecting said host arithmetic operation processing block and said plurality of digital signal processing blocks, and

Fig. 1


101
TUNER
102
DEMUX
103
VIDEO DECODER
104
AUDIO DECODER
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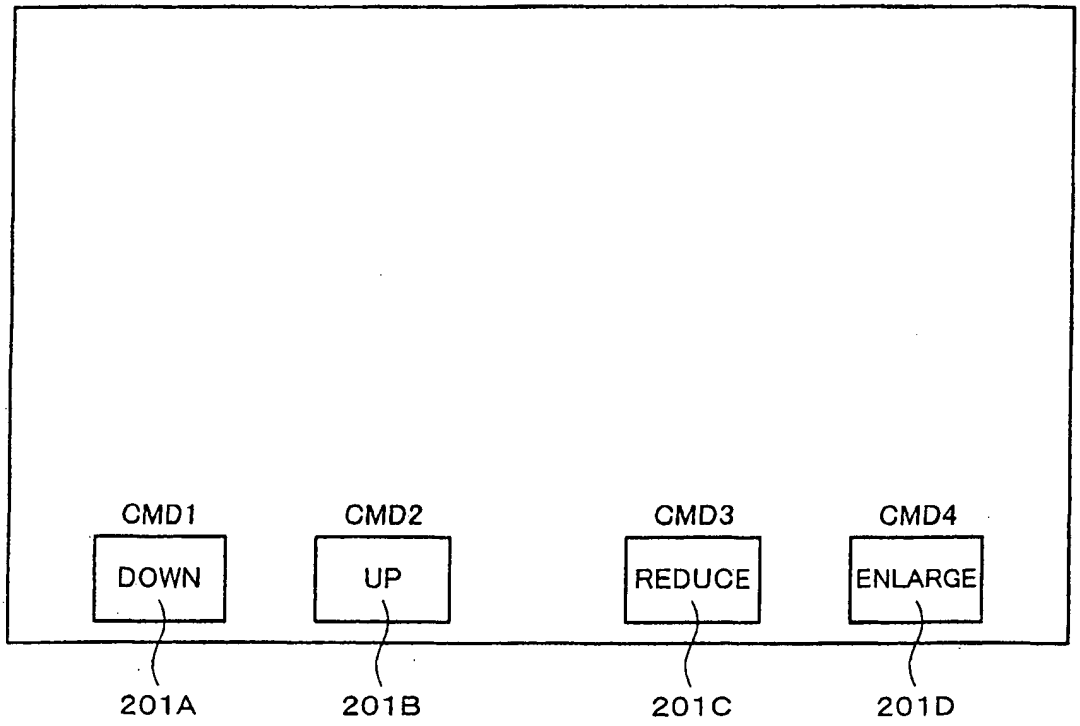
GRAPHICS
106
107
108
MODEM
112
MPU
111
IEEE1394 I/F
113
110

Fig. 3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DOWN
CMD2
UP
CMD3
REDUCE
CMD4
ENLARGE
201A
201B
201C
201D

Fig. 6

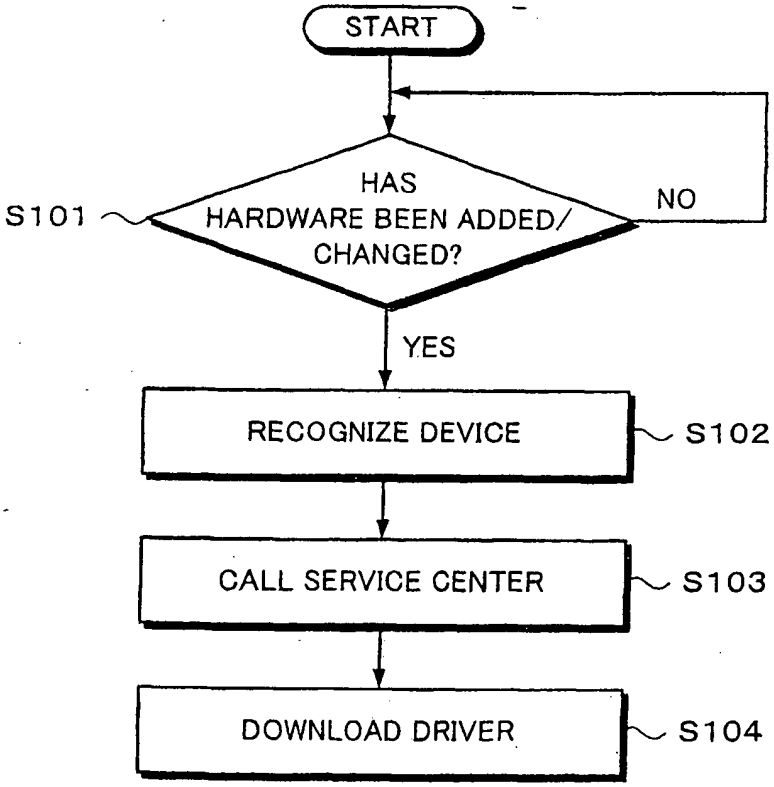
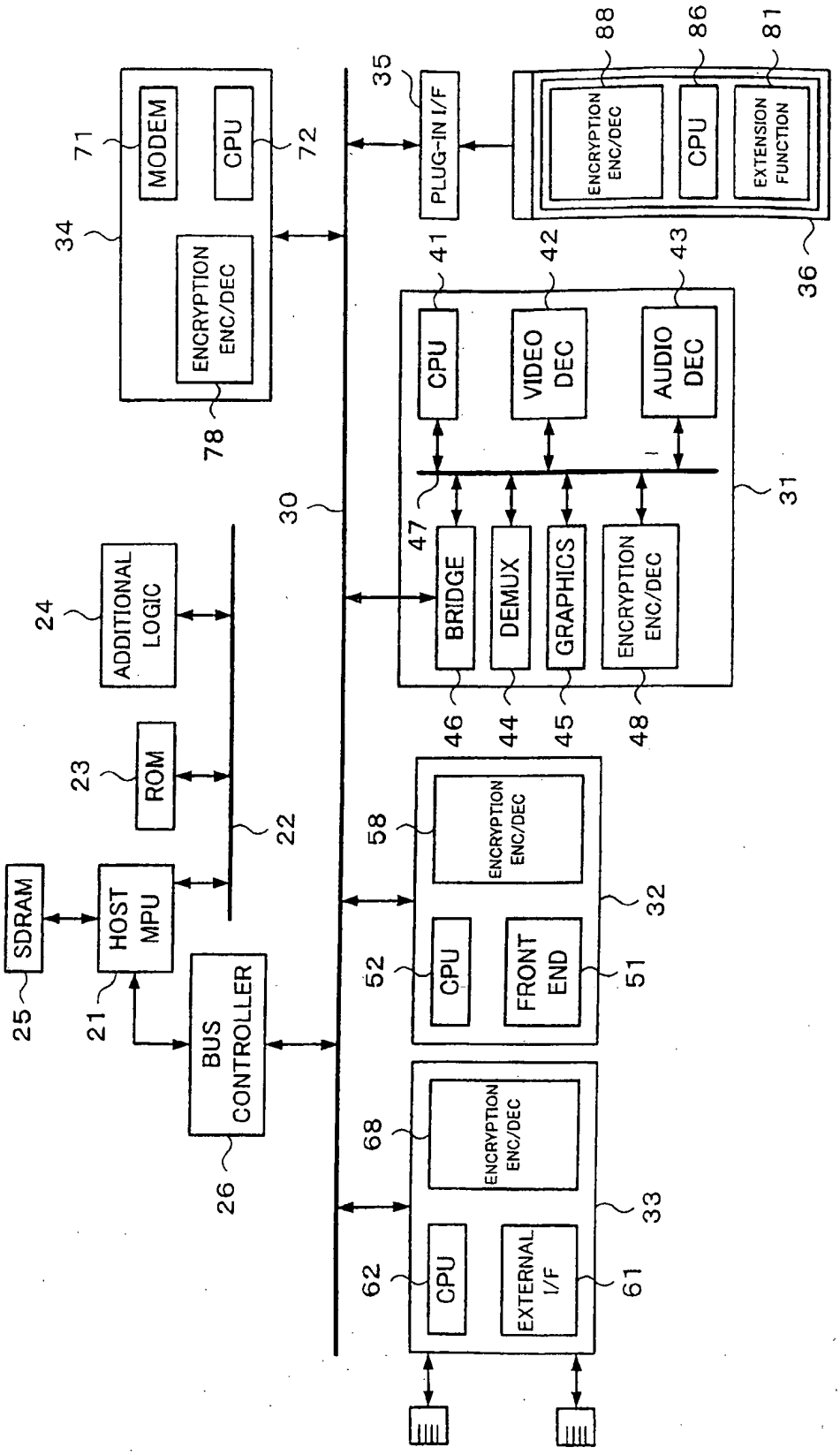

START
HAS HARDWARE BEEN ADDED/ CHANGED?
S101
NO
YES
RECOGNIZE DEVICE
S102
CALL SERVICE CENTER
S103
DOWNLOAD DRIVER
S104

Fig. 8


SDRAM
HOST MPU
ROM
ADDITIONAL LOGIC
BUS CONTROLLER
MODEM
CPU
ENCRYPTION ENC/DEC
PLUG-IN I/F
ENCRYPTION ENC/DEC
CPU
EXTENSION FUNCTION
CPU
VIDEO DEC
AUDIO DEC
BRIDGE
DEMUX
GRAPHICS
ENCRYPTION ENC/DEC
ENCRYPTION ENC/DEC
CPU
FRONT END
ENCRYPTION ENC/DEC
CPU
EXTERNAL I/F
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88

Fig. 10

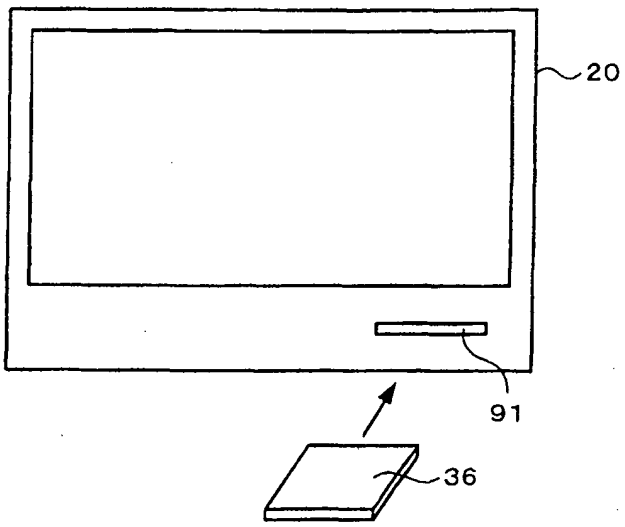


Fig. 12

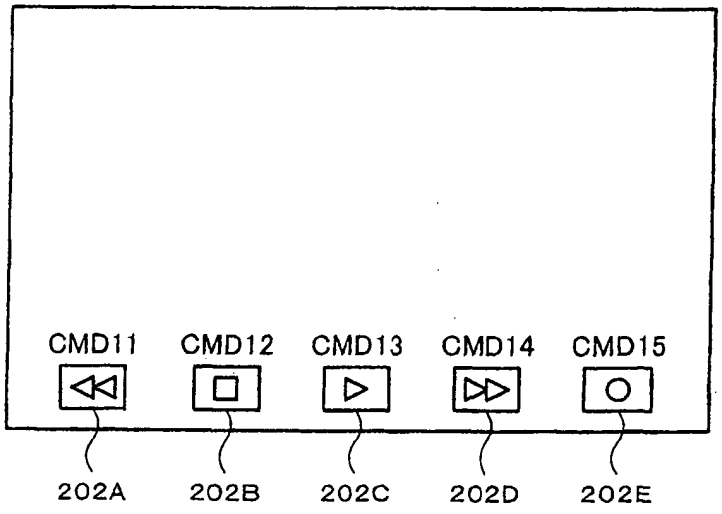
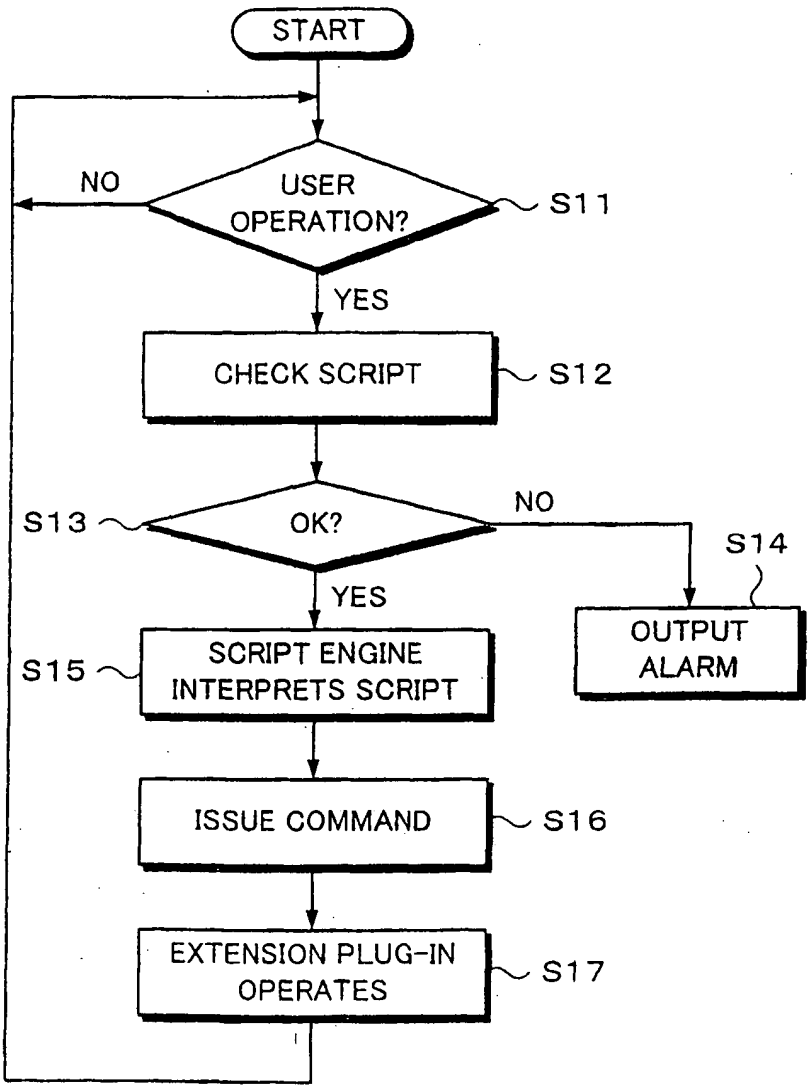


Fig. 14


START
USER OPERATION?
NO
S11
YES
CHECK SCRIPT
S12
OK?
S13
NO
S14
YES
OUTPUT ALARM
SCRIPT ENGINE INTERPRETS SCRIPT
S15
ISSUE COMMAND
S16
EXTENSION PLUG-IN OPERATES
S17

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP00/08113

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H04N5/44

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H04N5/44, H04L12/28-46

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Toroku Jitsuyo Shinan Koho 1994-2001
Kokai Jitsuyo Shinan Koho 1971-2001 Jitsuyo Shinan Toroku Koho 1996-2001

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP, 8-79641, A (Toshiba Corporation), 22 March, 1996 (22.03.96), Full text & EP, 700205, A & US, 5838383, A	1-12
Y	JP, 5-284524, A (Toshiba Corporation), 29 October, 1993 (29.10.93), Full text (Family: none)	1-12
Y	JP, 9-503108, A (Bell Communications Research Inc.), 25 March, 1997 (25.03.97), Full text & EP, 746920, A & US, 5600643, A	1-12

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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 January, 2001 (29.01.01)	13 February, 2001 (13.02.01)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)